FIG. 1

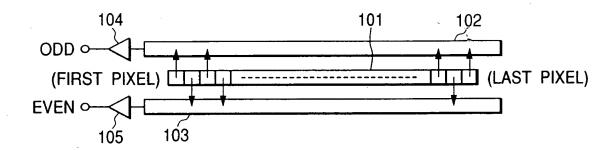
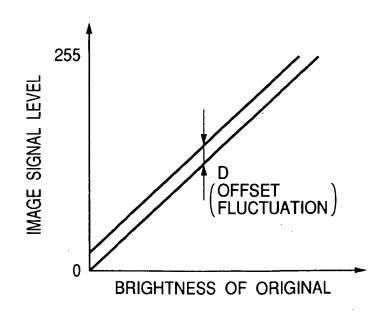


FIG. 2



F/G. 3

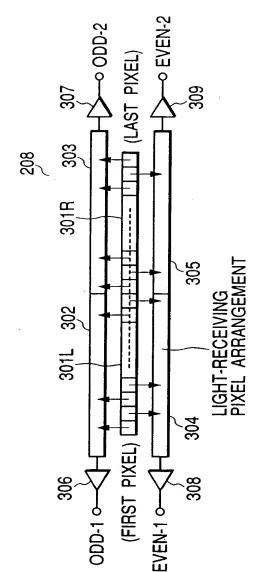
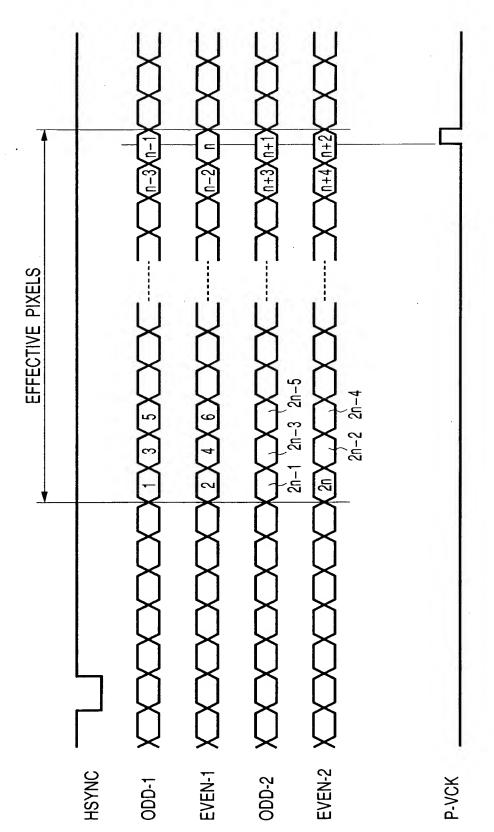


FIG. 4





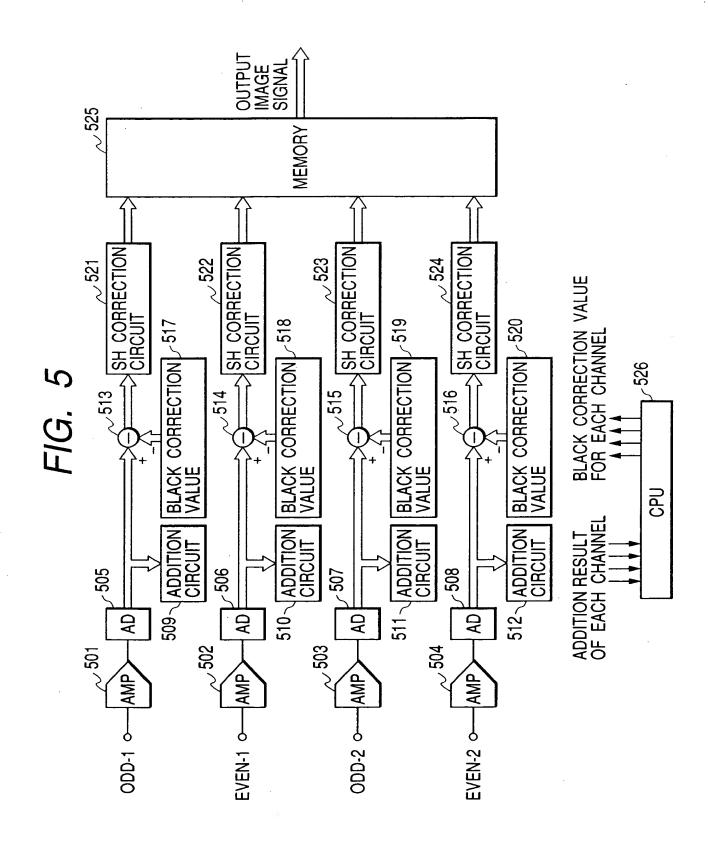
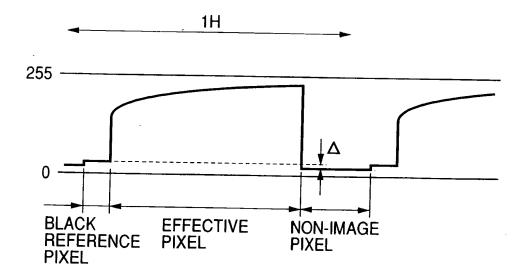


FIG. 6



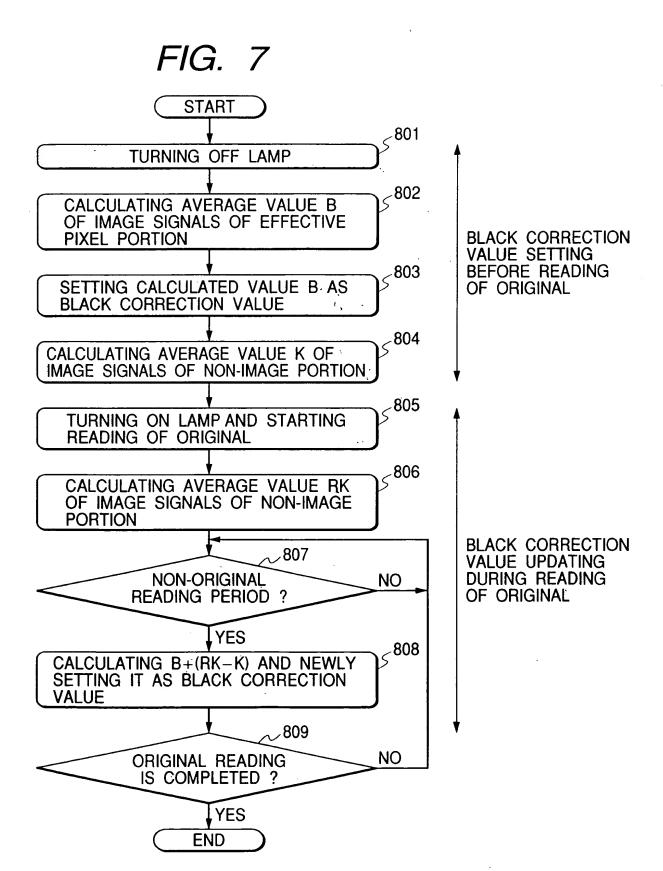
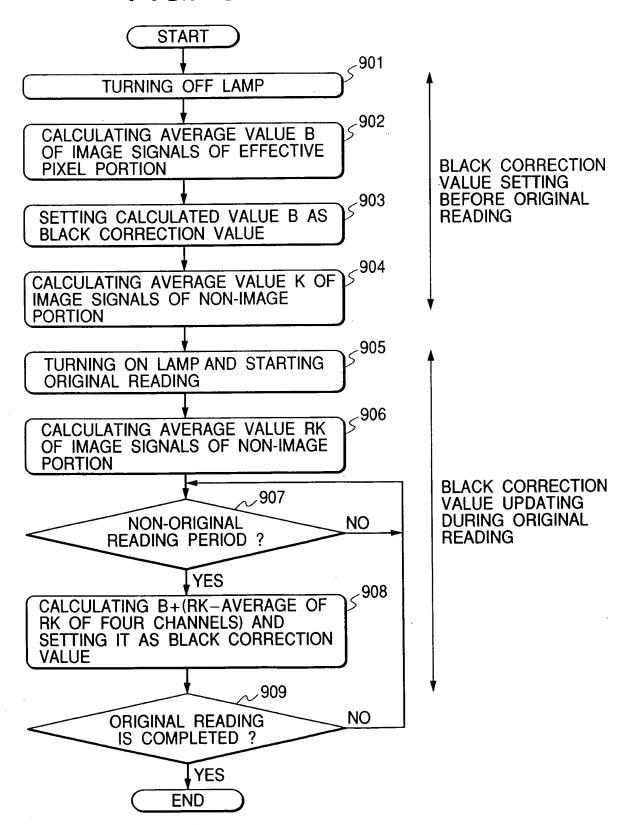


FIG. 8



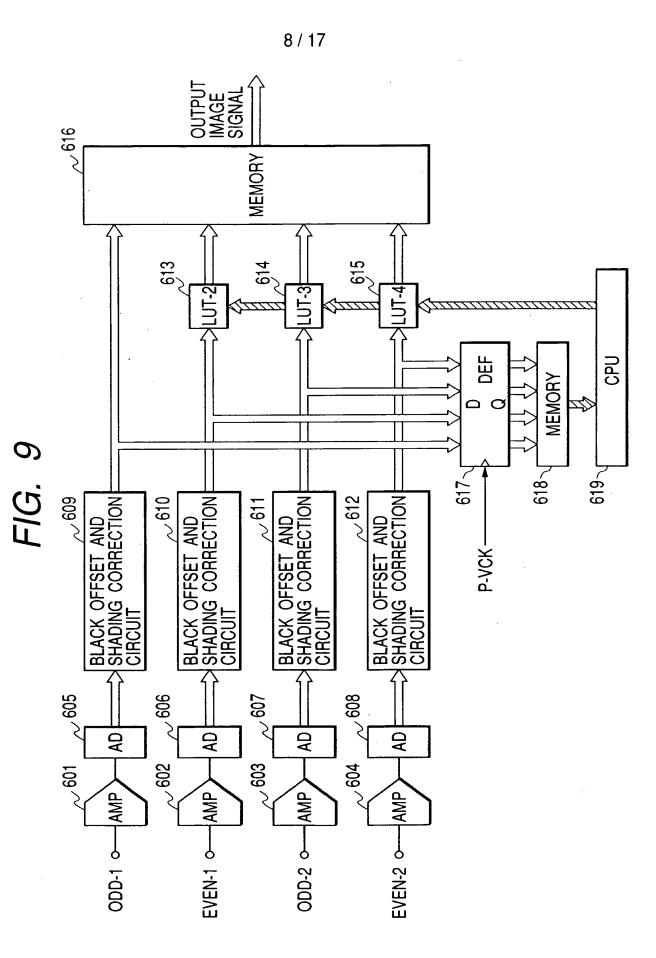


FIG. 10

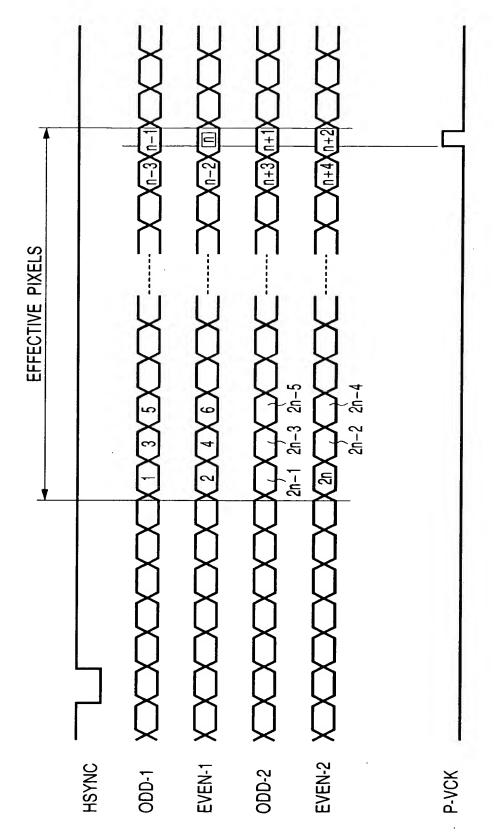


FIG. 11A

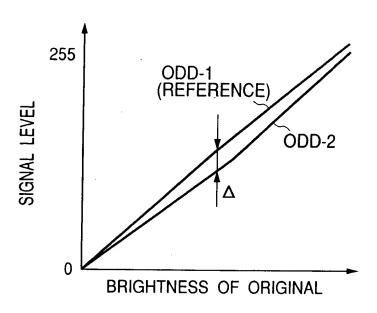


FIG. 11B

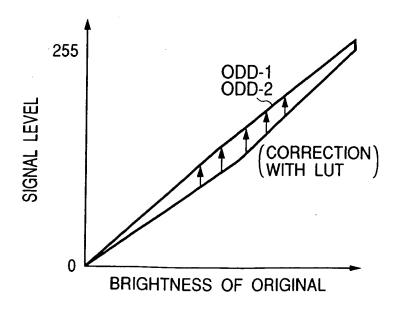


FIG. 12

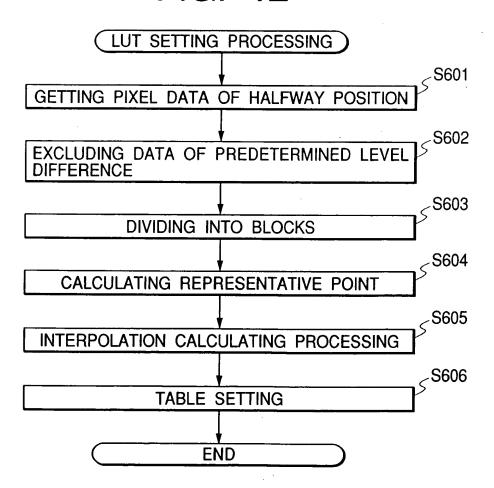


FIG. 13

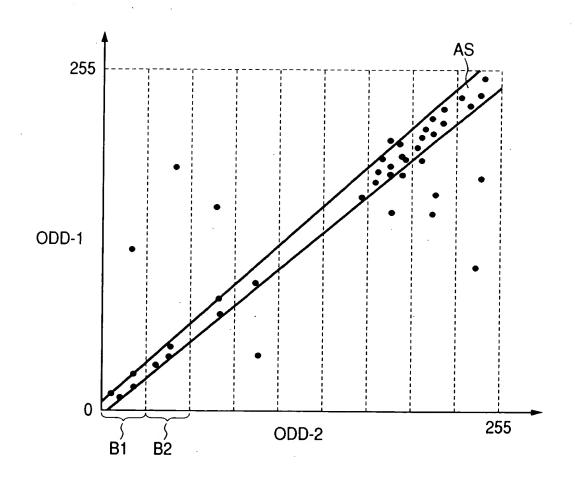


FIG. 14

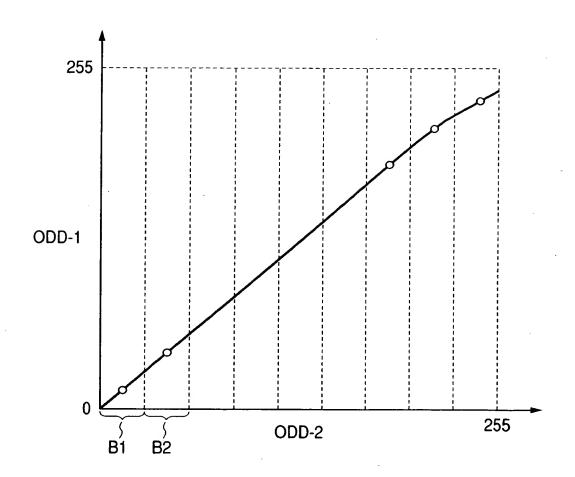
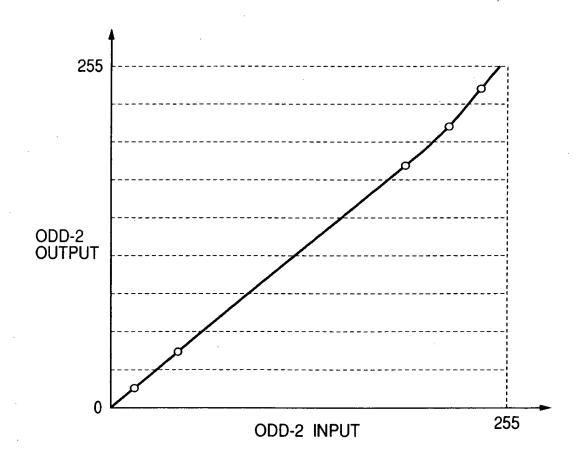
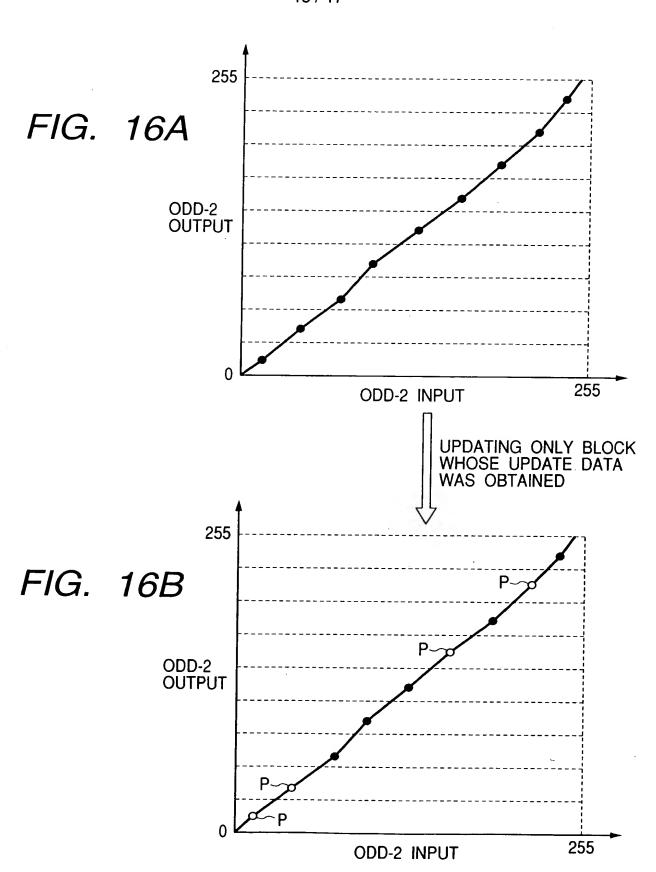


FIG. 15





8 bit \sim 616 MEMORY 8 bit 8 bit 8 bit 8 bit 913 915 8 914 10 bit 10 bit 10 bit 10 bit DEF SPU MEMORY \Box FIG. 617 619 618 $609 \sim$ \sim 612 019 BLACK OFFSET AND SHADING CORRECTION CIRCUIT BLACK OFFSET AND SHADING CORRECTION CIRCUIT √611 BLACK OFFSET AND SHADING CORRECTION CIRCUIT 10 bit 10 bit 10 bit 10 bit 809 *∕* ,605 909 ~ 607 AD <u>AD </u> AD AD **605** \sim 604 ,603 601 AMP AMP AMP AMP EVEN-2 O-EVEN-1

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FIG. 18

